```
=> s 395/?/ccls
L1        25460 395/?/CCLS

=> s l1 and (microprocessor? (p) (dual (w) clock?))
            84534 MICROPROCESSOR?
           133036 DUAL
           275558 CLOCK?
               32 MICROPROCESSOR? (P) (DUAL (W) CLOCK?)
L2              7 L1 AND (MICROPROCESSOR? (P) (DUAL (W) CLOCK?))

=> d l2 kwic 1-7
```

US PAT NO: 5,659,703 [IMAGE AVAILABLE] L2: 1 of 7
US-CL-CURRENT: 711/109; **395/800.42**

DETDESC:

DETD(176)

Most **microprocessors** derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The **microprocessor** 50 provides a **dual**-**clock** scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory. . . . vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the **microprocessor** 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the. . . of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the **microprocessor** 50 and acknowledges the presence of I/O data. The **microprocessor** 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another. . .

US PAT NO: 5,604,915 [IMAGE AVAILABLE] L2: 2 of 7
US-CL-CURRENT: **395/880**; 364/238.4, 942.1, DIG.1, DIG.2

DETDESC:

DETD(175)

Most **microprocessors** derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The **microprocessor** 50 provides a **dual**-**clock** scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory. . . . vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the **microprocessor** 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the. . . of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the **microprocessor** 50 and acknowledges the presence of I/O data. The **microprocessor** 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another. . .

US PAT NO: 5,530,890 [IMAGE AVAILABLE] L2: 3 of 7
US-CL-CURRENT: **395/800.32**; 364/232.8, 244.3, 931, 937.1, 965.4, DIG.1, DIG.2

DETDESC:

DETD(174)

Most **microprocessors** derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The **microprocessor** 50 provides a **dual**-**clock** scheme as shown inFIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller. . . may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronizedto the **microprocessor** 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the. . . of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the **microprocessor** 50 and acknowledges the presence of I/O data. The **microprocessor** 50 fetches up to four instructions in a single memory cycleand can perform much useful work before requiring another memory. . .

US PAT NO: 5,440,749 [IMAGE AVAILABLE] L2: 4 of 7
US-CL-CURRENT: **395/382**; 364/232.8, 244.3, 926.6, 931, 937.1, 965.4, DIG.1, DIG.2

DETDESC:

DETD(174)

Most **microprocessors** derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The **microprocessor** 50 provides a **dual**-**clock** scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory. . . vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the **microprocessor** 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the. . . of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the **microprocessor** 50 and acknowledges the presence of I/O data. The **microprocessor** 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another. . .

US PAT NO: 4,553,224 [IMAGE AVAILABLE] L2: 5 of 7
US-CL-CURRENT: **395/825**; 364/926.9, 926.92, 927.92, 927.99, 929.1, 929.2, 929.4, 929.5, 929.61, 933.2, 934, 935.2, 935.4, 935.45, 935.46, 938, 940, 942, 942.3, 942.51, 942.8, 946.2, 946.5, 949, DIG.2

DETDESC:

DETD(37)

The . . . an OR gate 118 that couples the force error line 73 and the read line 38 to one of the **dual** **clock** inputs on a watchdog timer 119. The timer 119 includes a monostable multivibrator and an RC coupling circuit for determining the timing constant. A reset line 120 coming from the **microprocessor** 20 is connected to the other clock input of the timer 119 and to a reset terminal on the watchdog. . .

US PAT NO: 4,302,820 [IMAGE AVAILABLE] L2: 6 of 7
US-CL-CURRENT: **395/598**; 364/920.4, 921, 921.3, 926, 926.9, 927.8, 929.1, 929.2, 938, 940, 940.1, 940.2, 940.3, 942.3, 942.8, 943, 943.1, 946.2, 946.9, 949, 950, 959.1, 964, 965, 965.5, DIG.2

DETDESC:

DETD(39)

The . . . an OR gate 118 that couples the force error line 73 and the read line 38 to one of the **dual clock** inputs on a watchdog timer 119. The timer 119 includes a monostable multivibrator and an RC coupling circuit for determining the timing constant. A reset line 120 coming from the **microprocessor** 20 is connected to the other clock input of the timer 119 and to a reset terminal on the watchdog. . .

US PAT NO: 4,293,924 [IMAGE AVAILABLE] L2: 7 of 7
US-CL-CURRENT: **395/834**; 364/921, 921.4, 926, 926.9, 927.8, 927.82, 927.92, 927.99, 929.2, 929.4, 931, 931.4, 937, 938, 938.1, 940, 940.1, 940.2, 942, 942.06, 942.8, 949, 959.1, 964, 965, 965.5, DIG.2

DETDESC:

DETD(36)

The . . . includes an OR gate 118 that couples the FORCE line 73 and the read line 38 to one of the **dual clock** inputs on a watchdog timer 119. The timer 119 includes a monostable multivibrator and an RC coupling circuit for determining the timing constant. A reset line 120 coming from the **microprocessor** 20 is connected to the other clock input of the timer 119 and to a reset terminal on the watchdog. . .

=>

=> d his

(FILE 'USPAT' ENTERED AT 08:09:56 ON 23 APR 1998)
SET PAGE SCROLL
L1 25460 S 395/?/CCLS
L2 7 S L1 AND (MICROPROCESSOR? (P) (DUAL (W) CLOCK?))
L3 5 S L1 AND (PROCESSOR (P) (DUAL (W) CLOCK?))

=> d l2 1-7

1. 5,659,703, Aug. 19, 1997, Microprocessor system with hierarchical stack and method of operation; Charles H. Moore, et al., 711/109; **395/800.42** [IMAGE AVAILABLE]

2. 5,604,915, Feb. 18, 1997, Data processing system having load dependent bus timing; Charles H. Moore, et al., **395/880**; 364/238.4, 942.1, DIG.1, DIG.2 [IMAGE AVAILABLE]

3. 5,530,890, Jun. 25, 1996, High performance, low cost microprocessor; Charles H. Moore, et al., **395/800.32**; 364/232.8, 244.3, 931, 937.1, 965.4, DIG.1, DIG.2 [IMAGE AVAILABLE]

4. 5,440,749, Aug. 8, 1995, High performance, low cost microprocessor architecture; Charles H. Moore, et al., **395/382**; 364/232.8, 244.3, 926.6, 931, 937.1, 965.4, DIG.1, DIG.2 [IMAGE AVAILABLE]

5. 4,553,224, Nov. 12, 1985, Multiplexed data handler for programmable controller; Odo J. Struger, et al., **395/825**; 364/926.9, 926.92, 927.92, 927.99, 929.1, 929.2, 929.4, 929.5, 929.61, 933.2, 934, 935.2, 935.4, 935.45, 935.46, 938, 940, 942, 942.3, 942.51, 942.8, 946.2, 946.5, 949, DIG.2 [IMAGE AVAILABLE]

6. 4,302,820, Nov. 24, 1981, Dual language programmable controller; Odo J. Struger, et al., **395/598**; 364/920.4, 921, 921.3, 926, 926.9, 927.8, 929.1, 929.2, 938, 940, 940.1, 940.2, 940.3, 942.3, 942.8, 943, 943.1, 946.2, 946.9, 949, 950, 959.1, 964, 965, 965.5, DIG.2 [IMAGE AVAILABLE]

7. 4,293,924, Oct. 6, 1981, Programmable controller with high density intelligent I/O interface; Odo J. Struger, et al., **395/834**; 364/921, 921.4, 926, 926.9, 927.8, 927.82, 927.92, 927.99, 929.2, 929.4, 931, 931.4, 937, 938, 938.1, 940, 940.1, 940.2, 942, 942.06, 942.8, 949, 959.1, 964, 965, 965.5, DIG.2 [IMAGE AVAILABLE]

=> d l3 1-5

1. 5,448,715, Sep. 5, 1995, Dual clock domain interface between CPU and memory bus; Charles A. Lelm, et al., **395/559** [IMAGE AVAILABLE]

2. 5,381,543, Jan. 10, 1995, **Processor** system with **dual** **clock**; James S. Blomgren, et al., **395/308**, **309** [IMAGE AVAILABLE]

3. 5,325,516, Jun. 28, 1994, **Processor** system with **dual** **clock**; James S. Blomgren, et al., 711/105; **395/309**, **551** [IMAGE AVAILABLE]

4. 4,450,525, May 22, 1984, Control unit for a functional processor; Gordon L. Demuth, et al., **395/590**; 364/221, 221.4, 221.5, 224, 224.2, 230, 230.3, 231.8, 238.4, 239, 239.1, 244, 244.3, 244.4, 244.6, 244.8, 247, 247.2, 254, 254.3, 254.5, 258, 258.1, 258.2, 259, 259.5, 260, 260.2, 261.3, 261.9, 262, 262.4, 262.8, 270.3, 280, 280.2, 281.3, DIG.1; **395/595**, **733** [IMAGE AVAILABLE]

5. 4,413,319, Nov. 1, 1983, Programmable controller for executing block transfer with remote I/O interface racks; Ronald E. Schultz, et al., **395/850**; 364/131, 221.9, 222, 222.2, 228, 228.5, 229, 229.2, 229.5, 230, 230.2, 230.5, 232.8, 238.3, 238.5, 238.6, 238.9, 239, 239.6, 239.7, 240, 240.2, 240.5, 240.8, 240.9, 241.9, 242.1, 242.5, 243, 243.7, 244, 244.1, 254, 254.3, 254.8, 259, 259.2, 259.3, 259.7, 260, 260.1, 264, 264.7, 267, 267.9, 271, 271.1, 280, 280.2, 280.8, 284, 284.1, 284.2, 284.3, 285, 285.4, DIG.1 [IMAGE AVAILABLE]

=>

```
=> s l1 and (processor (p) (dual (w) clock?))
        106977 PROCESSOR
        133036 DUAL
        275558 CLOCK?
            10 PROCESSOR (P) (DUAL (W) CLOCK?)
L3           5 L1 AND (PROCESSOR (P) (DUAL (W) CLOCK?))

=> d l3 kwic 1-5
```

US PAT NO: 5,448,715 [IMAGE AVAILABLE] L3: 1 of 5
US-CL-CURRENT: **395/559**

DETDESC:

DETD(4)

A **processor** chip interfaces through a **Dual Clock** Domain Interface (DCDI) to its associated memory and input/output devices via a memory bus. In a data store operation, the. . .

DETDESC:

DETD(10)

FIG. . . . block diagram of a computer system environment 101 in which the system and method of the present invention operate. A **processor** chip 114 interfaces through its on-chip **Dual Clock** Domain Interface (DCDI) 106 to its associated memory and input/output device(s) 110 via a variable frequency synchronous memory bus 108. This bus is the same bus used in existing PA-RISC **processor** designs. The **processor** 114 can be used with existing memory controllers, as well as future memory controller designs. This provides for a wide. . .

US PAT NO: 5,381,543 [IMAGE AVAILABLE] L3: 2 of 5
TITLE: **Processor** system with **dual clock**
US-CL-CURRENT: **395/308**, **309**

US PAT NO: 5,325,516 [IMAGE AVAILABLE] L3: 3 of 5
TITLE: **Processor** system with **dual clock**
US-CL-CURRENT: 711/105; **395/309**, **551**

US PAT NO: 4,450,525 [IMAGE AVAILABLE] L3: 4 of 5
US-CL-CURRENT: **395/590**; 364/221, 221.4, 221.5, 224, 224.2, 230, 230.3, 231.8, 238.4, 239, 239.1, 244, 244.3, 244.4, 244.6, 244.8, 247, 247.2, 254, 254.3, 254.5, 258, 258.1, 258.2, 259, 259.5, 260, 260.2, 261.3, 261.9, 262, 262.4, 262.8, 270.3, 280, 280.2, 281.3, DIG.1; **395/595**, **733**

ABSTRACT:
A control unit for a functional **processor** is disclosed which minimizes programming complexity by eliminating data transfers and the transfer control associated with two level memory systems. . . throughput of the combined operation of memory transfers, arithmetic processing and I/O transfers. In another feature, the controller employs a **dual clocking** arrangement whereby scratch pad storage elements and arithmetic elements can be selectively controlled to operate at twice the rate at. . .

US PAT NO: 4,413,319 [IMAGE AVAILABLE] L3: 5 of 5
US-CL-CURRENT: **395/850**; 364/131, 221.9, 222, 222.2, 228, 228.5, 229, 229.2, 229.5, 230, 230.2, 230.5, 232.8, 238.3, 238.5, 238.6, 238.9,

239, 239.6, 239.7, 240, 240.2, 240.5, 240.8, 240.9, 241.9, 242.1, 242.5, 243, 243.7, 244, 244.1, 254, 254.3, 254.8, 259, 259.2, 259.3, 259.7, 260, 260.1, 264, 264.7, 267, 267.9, 271, 271.1, 280, 280.2, 280.8, 284, 284.1, 284.2, 284.3, 285, 285.4, DIG.1

DETDESC:

DETD(140)

APPENDIX D

COMPONENT APPENDIX

Component	Ref. Nr.	Manufacturer's Chip Description
serial **processor**	31d	Z80A-CPU manufactured by Zilog, Inc.
parallel **processor**	31b	Z80A-CPU manufactured by Zilog, Inc.
I/O memory	31a	Two 6561 256-line .times. 4-bit random. . . transfer
memory	31c	Two 6561 256-line .times. 4-bit random access memories manufactured by Harris Corp.
serial **processor** program memory	S-PROM	Three 82S181 1k .times. 8-bit programmable read only memories manufactured by Signetics
parallel **processor** program memory	P-PROM	SN74S472 512-line .times. 8-bit programmable read only memory manufactured by Texas. . . receiver manufactured by Advanced Micro Devices, Inc.
four bit up/down counter	100	SN74LS193 up/down **dual clock** counter manufactured by Texas Instruments, Inc.
adapter **processor**	23b	Z80A-CPU manufactured by Zilog, Inc.
adapter counter/ timer circuit	A-CTC	Z80-CTC counter/ timer circuit. . .